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(56) Documents Cited
US 5600269 A US 5262686 A US 5182560 A

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(54) Abstract Title
A latching comparator for an analogue-to-digital converter

(57) Nodes VA and VB are precharged in one clock phase and then the comparator is enabled by transistor N5 in the other clock phase. The cross-coupled NMOS devices N0 and N1 respectively in parallel with the input transistors N2 and N3 improve switching speed. Placing the enabling transistor N5 at the tail of the circuit reduces clock-induced interference on the input nodes, which are floating during comparison.

FIG. 3

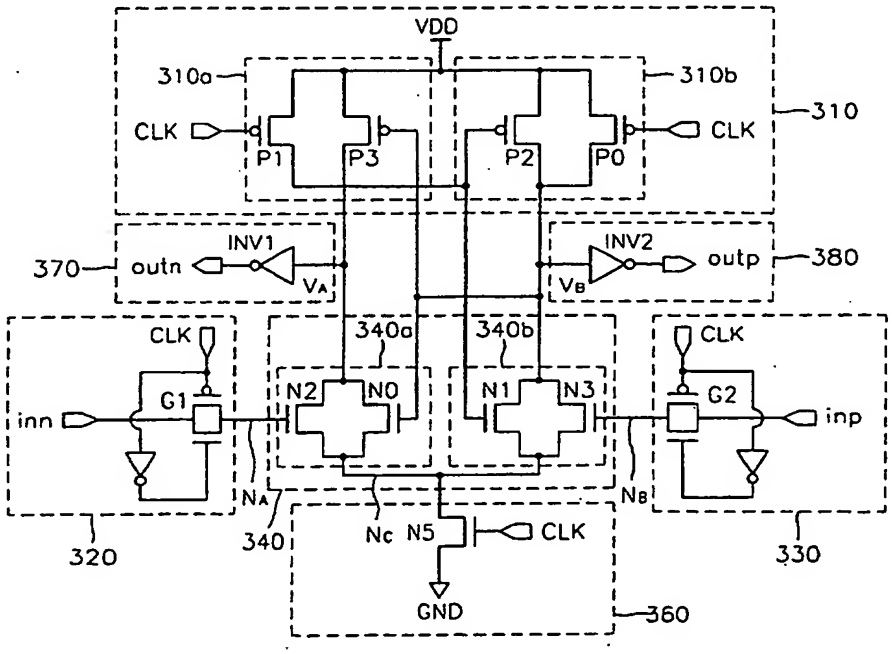

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FIG. 1 (PRIOR ART)

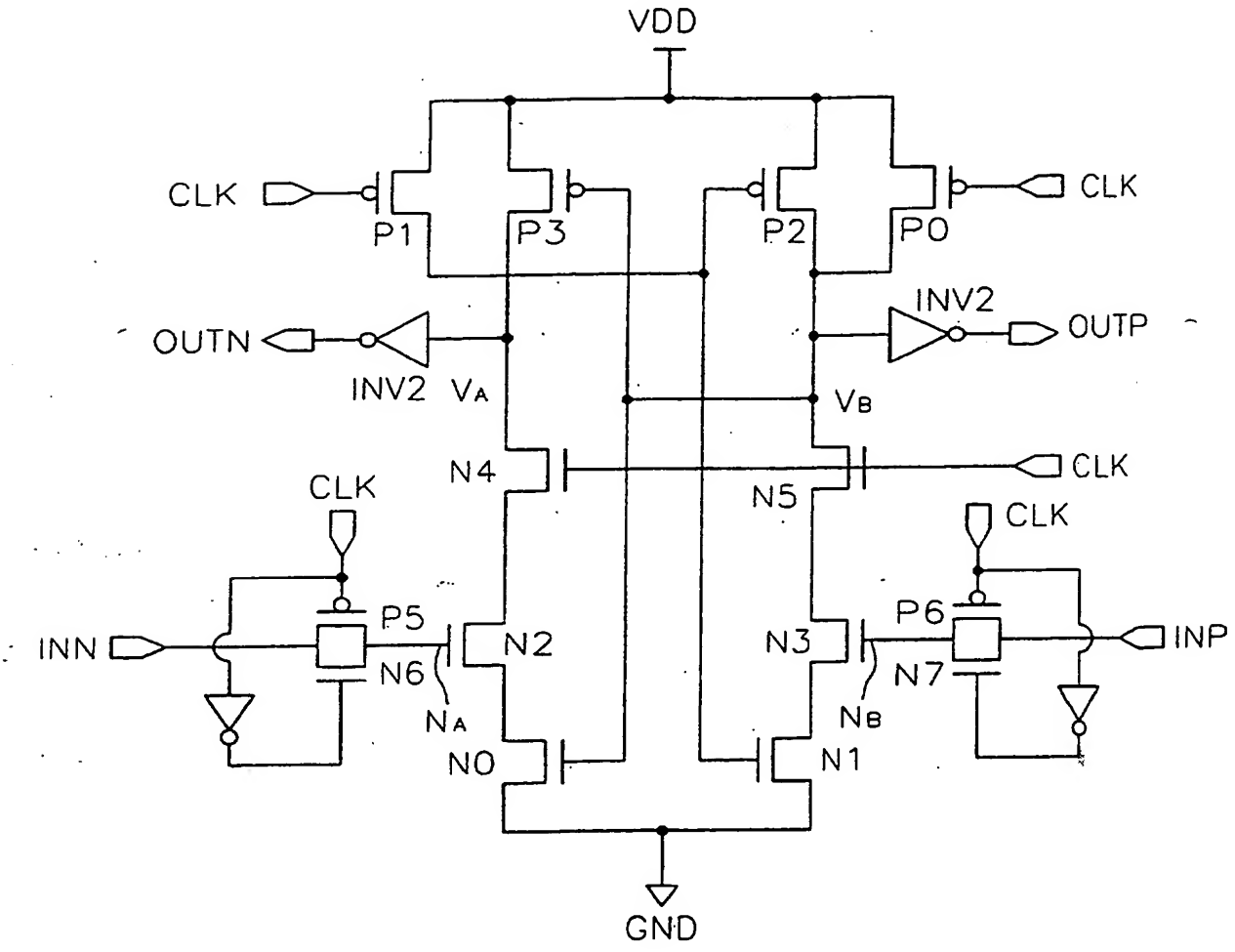


FIG. 2A (PRIOR ART)

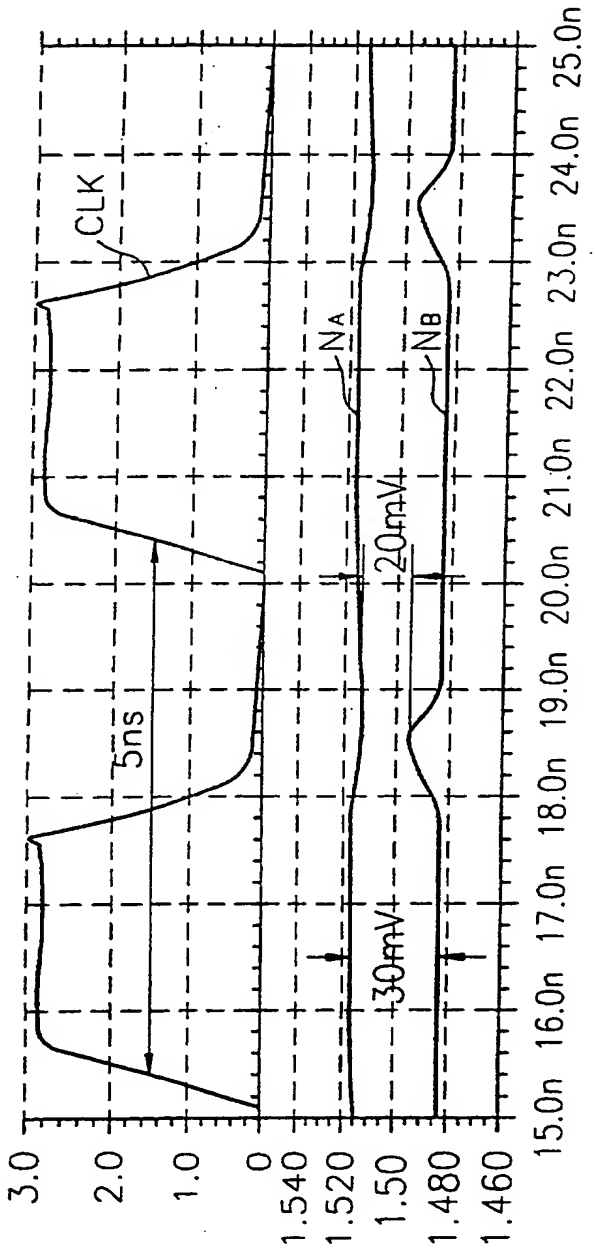


FIG. 2B (PRIOR ART)

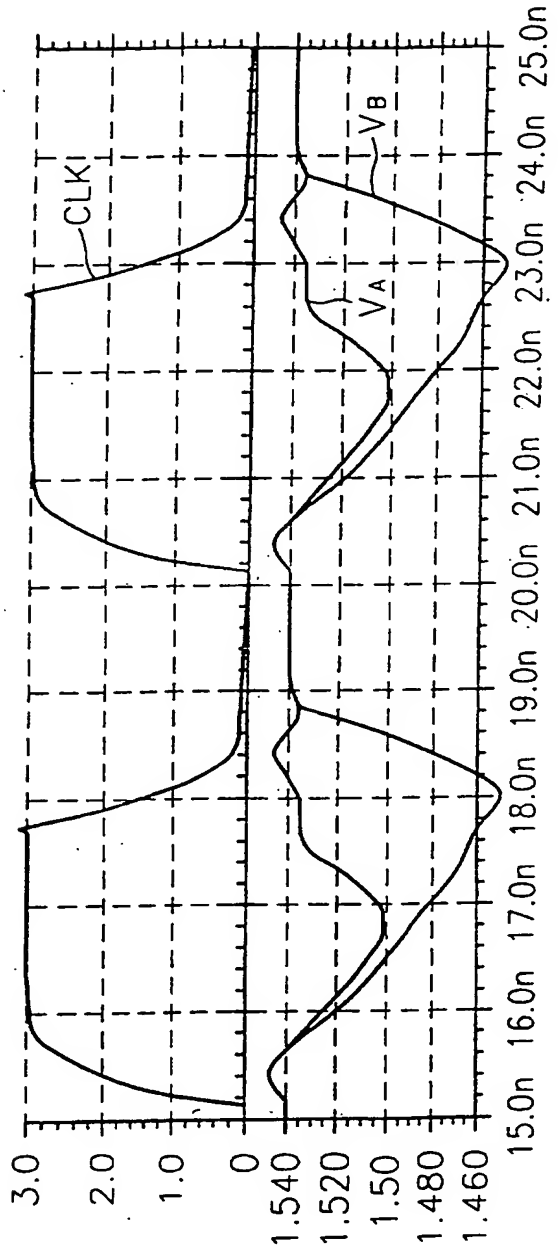


FIG. 3

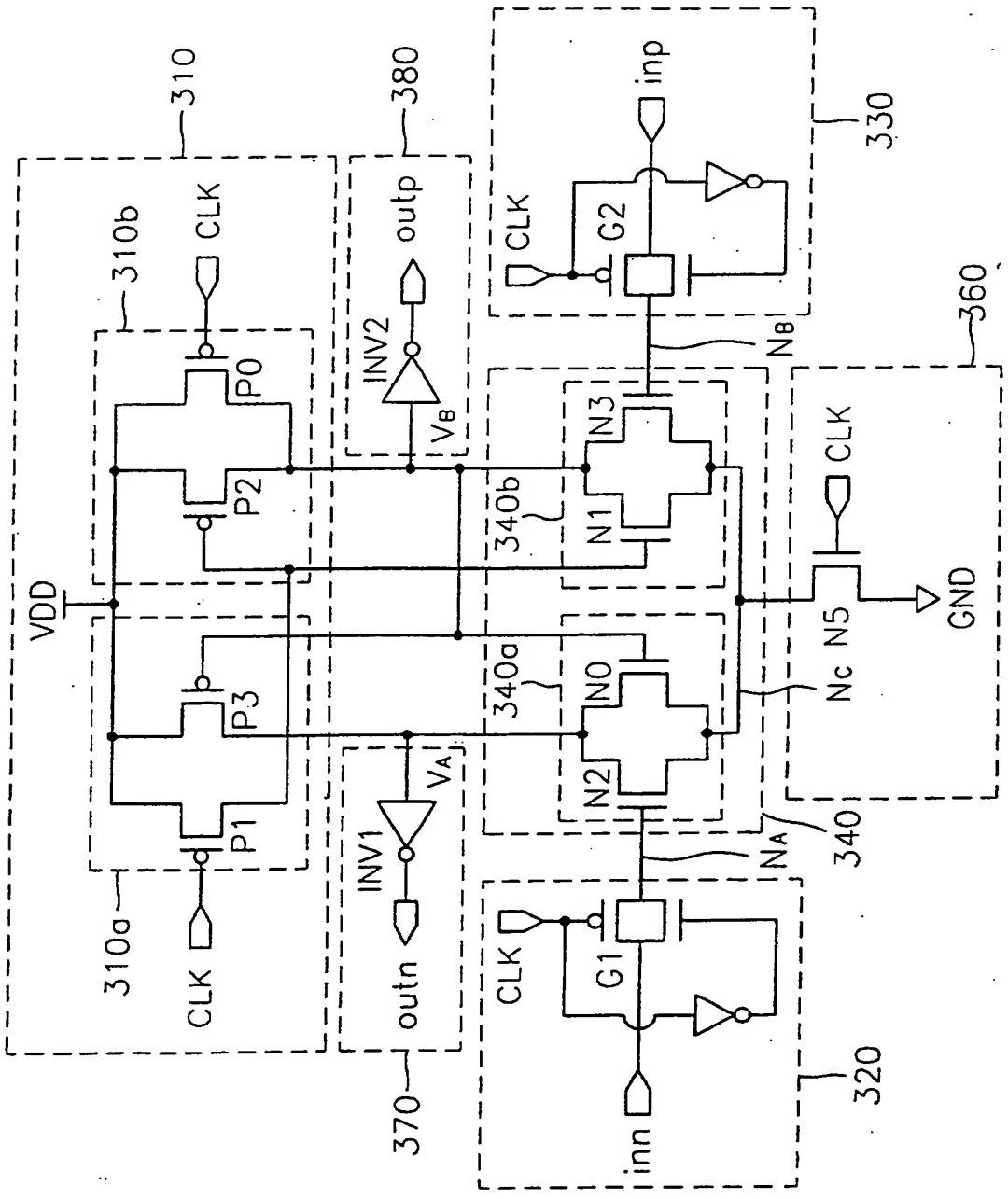


FIG. 4

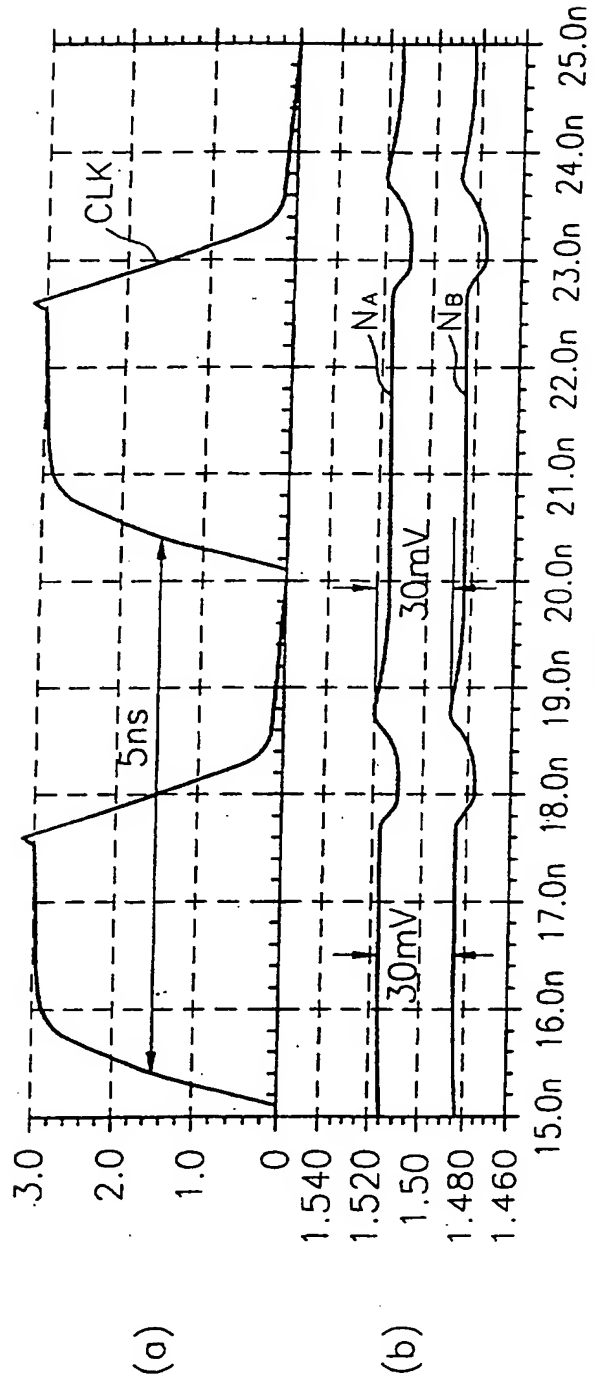
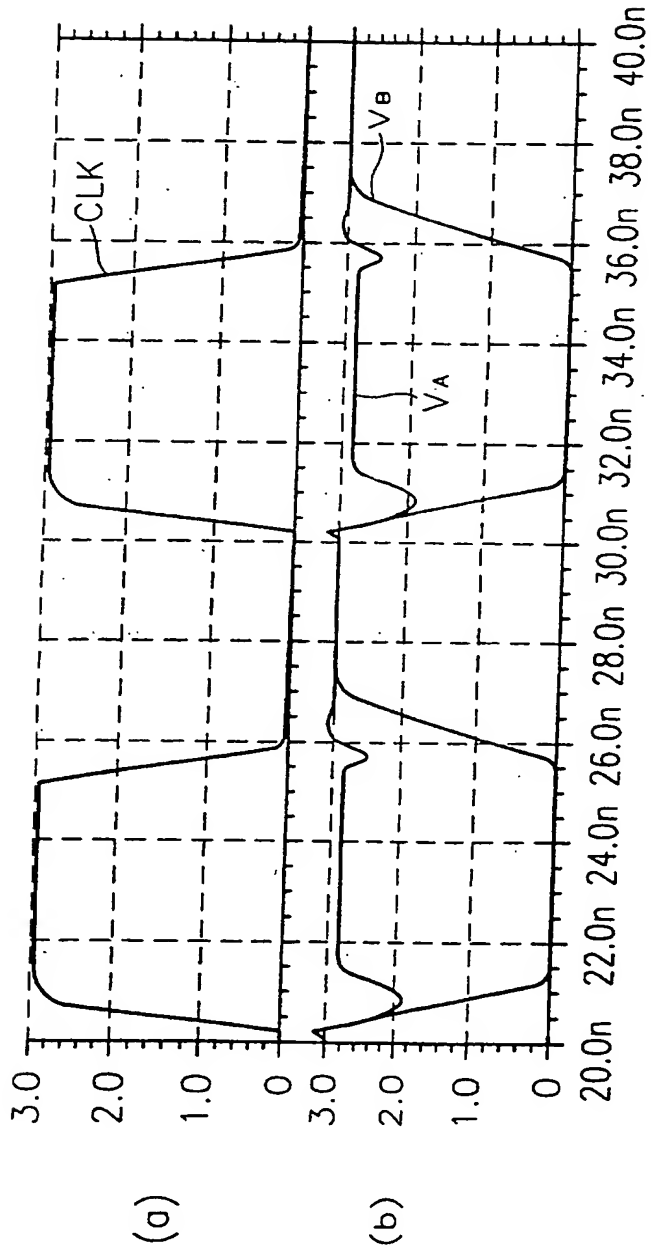


FIG. 5



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HIGH-SPEED DYNAMIC LATCH

The present invention relates to a high-speed dynamic latch, and more particularly, to a dynamic latch for a high-speed analog-to-digital (A/D) converter.

Generally, a latch is used for latching an address, data or internal clock signals for a given period, or maintaining a specific mode. When it comes to an A/D converter for a high definition television (HDTV) and a partial response maximum likelihood (PRML) method, a high-speed latch is required.

Figure 1 shows a conventional dynamic latch circuit. Referring to Figure 1, the latch circuit is operated in a track mode in which a clock signal CLK is in a logic low state and in a latch mode in which a clock signal CLK is in a logic high state. Specifically, when the latch circuit is in a track mode, PMOS transistors P0 and P1, NMOS transistors N4 and N5 pre-charge nodes V_A and V_B. Furthermore, PMOS transistors P2 and P3, and NMOS transistors N0 and N1 form an inverter latch. When the latch circuit is in a latch mode, two input signals INN and INP are latched to the logic high and the logic low states, respectively.

Firstly, when a clock signal CLK is logic low, NMOS transistors N4 and N5 are in a turned-off state while PMOS transistors P0 and P1 and input terminal switches P5 and P6 maintain a turned-on state. Therefore, nodes V_A and V_B become high, and the final output signals OUTN and OUTP which pass through inverters INV1 and INV2 remain "low".

In this case, an analog input signal is applied to the gate of NMOS transistors N2 and N3.

On the other hand, the moment that the clock signal CLK goes from logic low to logic high, the PMOS transistors P0 and P1 and the input terminal switches P5 and P6 turn off, and the NMOS transistors N4 and N5 turn on. Thus, electrical charges of the nodes V_A and V_B are each discharged through NMOS transistors N0 and N2, and N1 and N3, each pair of which is connected in series. In this case, a difference in the amount of current flowing in the NMOS transistors N2 and N3 is caused by the full differential input signals, i.e., signals of nodes N_A and N_B. Eventually, a voltage difference occurs between nodes V_A and V_B, and full differential output signals OUTN and OUTP are latched to the logic high and the logic low states, respectively, by an inverter latch consisting of PMOS transistors P2 and P3, and NMOS transistors N0 and N1.

Based on the foregoing, the latch circuit of Figure 1 removes static current consumption in a track mode. However, discharging is delayed in the latch circuit since NMOS transistors N0 and N2, and N1 and N3 are connected in series, respectively. Figure 2A depicts an analog input voltage difference between nodes N_A and N_B created by a clock signal CLK. Referring to Figure 2A, if the frequency of a clock signal CLK is 200 MHz (one clock cycle is 5 ns), a voltage difference between full differential input signals, i.e., signals of nodes V_A and V_B, is reduced by a kick-back voltage. This produces a problem in that it may effect the next clock cycle when a latch is operated at high speed.

Figure 2B shows the voltages of nodes V_A and V_B created by a clock signal CLK of 200 million samples per second (Msps). Referring to Figure 2B, NMOS transistors N2 and N3 are operated in a linear region during a latch mode, and NMOS transistors N2 and N0, and N3 and N1 are connected in series, which increases the required time for discharging. Therefore, the latch circuit has a drawback in that it cannot be used in a system requiring high-speed operation.

With a view to solve or reduce the above problems, it is an aim of embodiments of the present invention to provide a high-speed dynamic latch which removes kick-back voltage occurring in the existing latch and compensates for a drawback caused by low-speed charging/discharging.

According to a first aspect of the invention, there is provided a high-speed dynamic latch including: a first output node; a second output node; a precharging unit which precharges the first and second output nodes in response to a clock signal, a signal from the first output node, and a signal from the second output node; a discharging unit which discharges the first output node in parallel in response to one of a pair of differential input signals and a signal from the second output node, and discharges the second output node in parallel in response to the other of the pair of differential input signals and a signal from the first output node; and a current source which sinks current from the discharging unit in response to the clock signal.

The high-speed dynamic latch preferably further comprises: a first input unit which receives one of the

pair of differential input signals in response to the clock signal; and a second input unit which receives the other of the pair of differential input signals in response to the clock signal.

The high-speed dynamic latch may further comprise: a first output unit which inverts the signal from the first output node to output the inverted result; and a second output unit which inverts the signal from the second output node to output the inverted result.

Preferably, the precharging unit comprises: a first precharging unit which precharges the first output node in response to the clock signal and the signal from the second output node; and a second precharging unit which precharges the second output node in response to the clock signal and the signal from the first output node.

Preferably, the discharging unit comprises: a first discharging unit which discharges the first output node in parallel, in response to one of the pair of differential input signals and the signal from the second output node; and a second discharging unit which discharges the second output node in parallel, in response to the other of the pair of differential input signals and the signal from the first output node.

Preferably, the first precharging unit comprises: a first MOS transistor having a source connected to a first reference voltage node, a gate connected to the clock signal, and a drain connected to the first output node; and a second MOS transistor having a source connected to the first reference voltage node, a gate connected to the

second output node, and a drain connected to the first output node.

Preferably, the second precharging unit comprises: a first MOS transistor having a source connected to a first reference voltage node, a gate connected to the clock signal, and a drain connected to the second output node; and a second MOS transistor having a source connected to the first reference voltage node, a gate connected to the first output node, and a drain connected to the second output node.

Preferably, the first discharging unit comprises: a first MOS transistor having a drain connected to the first output node, a gate connected to one of the pair of differential input signals, and a source connected to a common node; and a second MOS transistor having a drain connected to the first output node, a gate connected to the second output node, and a source connected to the common node.

Preferably, the second discharging unit comprises: a first MOS transistor having a drain connected to the second output node, a gate connected to the other of the pair of differential input signals, and a source connected to a common node; and a second MOS transistor having a drain connected to the second output node, a gate connected to the first output node, and a source connected to the common node.

The current source may be connected between the discharging unit and a second reference voltage node, and

comprises a MOS transistor to the gate of which the clock signal is applied.

For a better understanding of the invention, and to show how embodiments of the same may be carried into effect, reference will now be made, by way of example, to the accompanying diagrammatic drawings in which:

Figure 1 shows a conventional dynamic latch circuit;

Figures 2A and 2B are graphs showing the simulation results of the circuit of Figure 1;

Figure 3 shows a dynamic latch circuit according to the present invention;

Figure 4 is a graph showing the simulation results of Figure 3; and

Figure 5 is a graph showing the simulation results with respect to the discharge time of Figure 3.

Referring to Figure 3, which shows a dynamic latch circuit according to the present invention, the dynamic latch circuit includes a precharging unit 310, a discharging unit 340, a current source 360, first and second input units 320 and 330, and first and second output unit 370 and 380. The precharging unit 310 precharges a first output node V_A and a second output node V_B in response to a clock signal CLK, a signal from the first output node V_A, and a signal from the second output node V_B. The discharging unit 340 discharges a first output node V_A in parallel in response to one of a pair of

differential input signals, i.e., a signal of node N_A, and a signal from the second output node V_B, and discharges the second output node V_B in parallel in response to the other differential input signal, i.e., a signal of node N_B, and a signal from the first output node V_A.

The current source 360 sinks current from the discharging unit 340 in response to a clock signal CLK. The first input unit 320 transmits a first input signal INN to a node N_A in response to the clock signal CLK. The second input unit 330 transmits a second input signal INP to a node N_B in response to a clock signal CLK.

The first and second input signals INN and INP are differential input signals, and thus signals of the node N_A and the node N_B are the differential input signals. The first output unit 370 inverts a signal from the first output node V_A to output the result as a first output signal OUTN. The second output unit 380 inverts a signal from the second output node V_B to output the result as a second output signal OUTP.

More specifically, the precharging unit 310 is divided into first and second precharging units 310a and 30b. The first precharging unit 310a includes a PMOS transistor P1 having a source connected to a first reference voltage node, i.e. power voltage node V_{DD}, a gate connected to a clock signal CLK, and a drain connected to the first output node V_A; and a PMOS transistor P3 having a source connected to the first reference voltage node V_{DD}, a gate connected to the second output node V_B, and a drain connected to the first output node V_A. The second precharging unit 310b includes a PMOS transistor P0 having a source connected to the first reference voltage node

V_{DD}, a gate connected to a clock signal CLK, and a drain connected to the second output node V_B; and a PMOS transistor P2 having a source connected to the first reference voltage node V_{DD}, a gate connected to the first output node V_A, and a drain connected to the second output node V_B.

The discharging unit 340 is divided into first and second discharging units 340a and 340b. The first discharging unit 340a includes an NMOS transistor N2 having a drain connected to the first output node V_A, a gate connected to the other of the differential input signals, i.e., a signal at a node N_A, and a source connected to a node N_C; and an NMOS transistor N0 having a drain connected to the first output node V_A, a gate connected to the second output node V_B, and a source connected to a node N_C. The second discharging unit 340b includes an NMOS transistor N3 having a drain connected to the second output node V_B, a gate connected to the other of differential input signals, i.e., a signal at a node N_B, and a source connected to the node N_C; and an NMOS transistor N1 having a drain connected to the second output node V_B, a gate connected to the first output node V_A, and a source connected to the node N_C. The current source 360 is connected between a node N_C and a second reference voltage node, i.e., ground voltage node GND, and includes an NMOS transistor N5 to the gate of which a clock signal CLK is applied.

The detailed circuit operation will now be described with reference to Figure 3. Firstly, during a track mode in which a clock signal CLK is at logic low, the NMOS transistor N5 is in a turned-off state, and the PMOS

transistors P1 and P0 of the precharging unit 310, and transmission gates G1 and G2 of the first and second input units 320 and 330 maintain a turned-on state. Thus, the first and second output nodes V_A and V_B become "high", and the final output signals OUTN and OUTP passing through the inverters INV1 and INV2 of first and second output units 370 and 380 maintain a logic "low" level. In this case, analog differential input signals INN and INP are applied to the transmission gates G1 and G2 of the first and second input units 320 and 330.

During a latch mode in which a clock signal CLK goes logic low to logic high, the PMOS transistors P1 and P0, and the transmission gates G1 and G2 of the first and second input units 320 and 330 turn off, while the NMOS transistor N5 turns on. Thus, electrical charges of the first and second output nodes V_A and V_B begin to be discharged within the first and second discharging units 340a and 340b through the NMOS transistors N0 and N2, and N1 and N3 each pair of which is connected in parallel. In this case, a difference in the amount of current flowing in the NMOS transistors N2 and N3 is caused by the full differential input signals, i.e., signals of nodes N_A and N_B. Therefore, a voltage difference occurs between the first and second output nodes. This causes an inverter latch comprised of the PMOS transistors P2 and P3, and NMOS transistors N0 and N1 to latch full differential output signals OUTN and OUTP passing through the inverters INV1 and INV2 to a logic high and a logic low states, respectively.

Furthermore, the NMOS transistor N5 for controlling precharge and discharge of the output nodes V_A and V_B is

commonly connected to the sources of NMOS transistors N0, N1, N2, and N3 within the discharging unit 340, which prevents a restriction in a high-speed operation caused by kick-back voltage.

Figure 4 is a graph showing the simulation result with respect to kick-back voltage of the dynamic latch circuit of Figure 3. Figure 4(a) indicates a clock signal CLK of 200 million samples per second (Msps), and Figure 4(b) shows a voltage difference between full differential input signals, i.e., signals of the node N_A and the node N_B. As shown in Figure 4, a clock signal CLK affects analog input signals INN and INP by kick-back voltage. However, contrary to the existing latch shown in Figure 1, a voltage difference between full differential input signals, i.e., signals of the node N_A and the node N_B, is not reduced. Therefore, during high-speed operation, a voltage difference between analog input signals remains constant in each clock cycle.

Furthermore, the discharge time of output nodes V_A and V_B significantly affects high-speed operation. Generally, the falling and rising time of the two nodes are forced to be one half of the pulse width of operation frequency. In the dynamic latch circuit of Figure 3, the NMOS transistors N0 and N1 are connected in parallel to N2 and N3, respectively, instead of being connected in series like in the conventional one, which quickens the discharge time of output nodes V_A and V_B. Figures 5A and 5B are graphs showing the simulation results to the discharge time of nodes V_A and V_B in the circuit of Figure 3. Figure 5(a) indicates a clock signal CLK of 200 MHz, and Figure 5(b) is a voltage waveform of output nodes V_A and V_B. As shown in Figure 5, the discharge time of output

nodes V_A and V_B is about 1ns, so operation speed higher than 500 MHz can be obtained. In this case, the simulation of Figure 5 uses a 0.6 μm CMOS process model parameter.

As described above, the latch circuit according to the present invention is capable of removing kick-back voltage which may occur in the existing latch and compensating for a disadvantage resulting from low-speed charge/discharge, which improves its operation speed. Thus, the latch circuit according to the present invention can be used in a high-speed analog/digital converter of higher than 500 MHz.

The reader's attention is directed to all papers and documents which are filed concurrently with or previous to this specification in connection with this application and which are open to public inspection with this specification, and the contents of all such papers and documents are incorporated herein by reference.

All of the features disclosed in this specification (including any accompanying claims, abstract and drawings), and/or all of the steps of any method or process so disclosed, may be combined in any combination, except combinations where at least some of such features and/or steps are mutually exclusive.

Each feature disclosed in this specification (including any accompanying claims, abstract and drawings), may be replaced by alternative features serving the same, equivalent or similar purpose, unless expressly stated otherwise. Thus, unless expressly stated otherwise,

each feature disclosed is one example only of a generic series of equivalent or similar features.

The invention is not restricted to the details of the foregoing embodiment(s). The invention extend to any novel one, or any novel combination, of the features disclosed in this specification (including any accompanying claims, abstract and drawings), or to any novel one, or any novel combination, of the steps of any method or process so disclosed.

CLAIMS

1. A high-speed dynamic latch comprising:

a first output node;

a second output node;

a precharging unit which precharges the first and second output nodes in response to a clock signal, a signal from the first output node, and a signal from the second output node;

a discharging unit which discharges the first output node in parallel in response to one of a pair of differential input signals and a signal from the second output node, and discharges the second output node in parallel in response to the other of the pair of differential input signals and a signal from the first output node; and

a current source which sinks current from the discharging unit in response to the clock signal.

2. The high-speed dynamic latch of claim 1, further comprising:

a first input unit which receives one of the pair of differential input signals in response to the clock signal; and

a second input unit which receives the other of the pair of differential input signals in response to the clock signal.

3. The high-speed dynamic latch of claim 1, further comprising:

a first output unit which inverts the signal from the first output node to output the inverted result; and

a second output unit which inverts the signal from the second output node to output the inverted result.

4. The high-speed dynamic latch of claim 1, 2 or 3, wherein the precharging unit comprises:

a first precharging unit which precharges the first output node in response to the clock signal and the signal from the second output node; and

a second precharging unit which precharges the second output node in response to the clock signal and the signal from the first output node.

5. The high-speed dynamic latch of claim 1, 2, 3 or 4, wherein the discharging unit comprises:

a first discharging unit which discharges the first output node in parallel, in response to one of the pair of differential input signals and the signal from the second output node; and

a second discharging unit which discharges the second output node in parallel, in response to the other of the pair of differential input signals and the signal from the first output node.

6. The high-speed dynamic latch of claim 4, wherein the first precharging unit comprises:

a first MOS transistor having a source connected to a first reference voltage node, a gate connected to the clock signal, and a drain connected to the first output node; and

a second MOS transistor having a source connected to the first reference voltage node, a gate connected to the second output node, and a drain connected to the first output node.

7. The high-speed dynamic latch of claim 4, wherein the second precharging unit comprises:

a first MOS transistor having a source connected to a first reference voltage node, a gate connected to the clock signal, and a drain connected to the second output node; and

a second MOS transistor having a source connected to the first reference voltage node, a gate connected to the first output node, and a drain connected to the second output node.

8. The high-speed dynamic latch of claim 5, wherein the first discharging unit comprises:

a first MOS transistor having a drain connected to the first output node, a gate connected to one of the pair of differential input signals, and a source connected to a common node; and

a second MOS transistor having a drain connected to the first output node, a gate connected to the second output node, and a source connected to the common node.

9. The high-speed dynamic latch of claim 5, wherein the second discharging unit comprises:

a first MOS transistor having a drain connected to the second output node, a gate connected to the other of the pair of differential input signals, and a source connected to a common node; and

a second MOS transistor having a drain connected to the second output node, a gate connected to the first output node, and a source connected to the common node.

10. The high-speed dynamic latch of any preceding claim, wherein the current source is connected between the discharging unit and a second reference voltage node, and comprises a MOS transistor to the gate of which the clock signal is applied.

11. A high-speed dynamic latch substantially as herein described with reference to Figures 3 to 5 of the accompanying drawings.

Application No:	GB 0028422.4	**Examiner:**	Keith Sylvan
Claims searched:	1-11	**Date of search:**	6 April 2001

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.S): H3P (PCT,PPTX)

Int Cl (Ed.7): H03K (3/356,5/24)

Other:

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
Y	US5600269	Song. See column 1 lines 5-13 and figures 9,11 and 12.	1-11
Y	US5262686	T.I. (Kurosawa) See column 1 lines 5-10 and figure 2.	1-11
Y	US5182560	T.I. (Shiwaku) See column 1 lines 14-17 and 625,626 in figure 6.	3

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.

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